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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/886,533	06/20/2001	Yajun Ha	IMEC214.001AUS	6391

20995 7590 07/05/2005

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EXAMINER	
KENDALL, CHUCK O	

ART UNIT	PAPER NUMBER
2192	

DATE MAILED: 07/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/886,533	HA ET AL.	
	Examiner	Art Unit	
	Chuck Kendall	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This action is in response to the application filed 04/04/05.

2. Claims 1 – 30 have been examined.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1 – 4, 21, 22, 27 & 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Shaylor USPN 6,760,907 B2.

Regarding claim 1, a method of transforming bytecode, the method comprising:

determining an abstract bytecode by performing a compilation of an application for execution on a virtual device (5:45 – 54);

transmitting the abstract bytecode from a service peer to at least a client peer (5:7 – 10);

transforming the received abstract bytecode into a native bytecode for a client specific device that is connected to the client peer, wherein the client specific device is configurable (5: 57 – 63);

configuring the client specific device using at least in part the native bytecode (5: 57 – 60, *for configuring* see convert to user specific type of hardware); and executing

the native bytecode at the client peer on the client specific device (5:61 – 64, see native executable).

Regarding claim 2, the method of claim 1, wherein the abstract bytecode comprises abstract hardware bytecode that includes configuration information of a virtual device (5:57 – 60, *for configuring* see convert to user specific type of hardware, also see figure 2, for virtual machine and hardware).

Regarding claim 3, the method of claim 1, wherein the abstract bytecode comprises abstract hardware bytecode and abstract software bytecode (figure 2, see hardware and virtual machine).

Regarding claim 4, the method of claim 1, wherein the abstract bytecode comprises abstract software bytecode and wherein transforming transforms the abstract software bytecode into native software bytecode that is executable on the client specific device (5: 55 – 60. for transform see convert).

Regarding claim 21, which recites similarly to claim 1, see reasoning as previously discussed above.

Regarding claim 22, which recites similarly to claim 1, see reasoning as previously discussed above.

Regarding claim 27, which recites the program storage version of claim 1, see reasoning as previously discussed above.

Regarding claim 30, which recites similarly to claim 1, see reasoning as previously discussed above.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5 –13, 16 – 20, 23, 24, & 28 are rejected under rejected under 35 U.S.C. 103(a) as being unpatentable over Shaylor USPN 6,760,907 B2 in view of Killian et al. USPN 6,477,683 B1.

Regarding claim 5, Shaylor discloses all the claimed limitations as applied in claim 4 above. Shaylor doesn't explicitly disclose wherein executing the application comprises configuring the configurable part of the client specific device and thereafter executing on the device. Shaylor does disclose converting byte code into user's specific type of hardware. Killian in an analogous art discloses a fully customizable synthesis script to be able to configure the particular FPGA (32:67 – 33: 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Shaylor and Killian because being able to configure the particular processor to the FPGA would make it more compatible and customizable.

Regarding claim 6, the method of claim 1, wherein the client specific device comprises a programmable logic device (Killian, 33:2 see FPGA).

Regarding claim 7, the method of claim 6, wherein the programmable logic device comprises a field programmable gate array (FPGA) (Killian, 33:2 see FPGA).

Regarding claim 8, Shaylor discloses all the claimed limitations as applied in claim 1 above. Shaylor doesn't explicitly disclose wherein the configurable part of the virtual device is modeled by a register transfer level description. Killian discloses in an analogous art discloses reading in all register transfer level files relevant to the specific processor configuration (33:7 – 10). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Shaylor and Killian, because using a register transfer level description would the processor the be more efficiently configured.

Regarding claim 9, Shaylor discloses all the claimed limitations as applied in claim 8 above. Shaylor doesn't explicitly disclose wherein the register transfer level description is a description of a datapath that includes a netlist of register transfer level datapath cores and a controller that is described by microcode. Killian in an analogous art disclose gate level netlists, which can be used with the FPGA (32:52 – 55).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Shaylor and Killian, because using a net list would enable register transfer level description to obtain CPLD implementations (Killian, 32: 52 – 57).

Regarding claim 10, Killian further discloses the method of claim 9, wherein transforming comprises:

selecting a physical core implementation for the datapath cores within the datapath description (40: 22 – 25, see datapath); and

generating connections between the selected datapath core implementations from the netlist within the datapath description (Killian, 40: 22 – 25, see datapath and hardware implementations).

Regarding claim 11, Killian further discloses the method of claim 10, wherein the datapath description provides a logic view for a plurality of physical core implementations, and wherein the datapath description and each of the physical core implementations have the same interface (Killian, 49:57 – 61.

Regarding claim 12, Shaylor discloses all the claimed limitations as applied in claim 1. Shaylor doesn't explicitly disclose, compiling the application and thereby generating abstract routing information and indicating in an abstract coordinate system, which channel segments are used for connecting ports of the abstract logic blocks, the abstract routing information being part of the abstract bytecode. Killian does disclose in an analogous art channels 212 to provide a communication link to PC hosts for downloading or debugging programs (32: 32 – 37). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Shaylor and Killian, because it would have enabled communication between the host and the system and made it more distributed.

Regarding claim 13, the method of claim 1, Killian further discloses wherein the configurable part of the virtual device comprises abstract logic blocks and an abstract

routing architecture that comprises channel segments for connecting part of the abstract logic blocks (Killian, 32: 32 – 37).

wherein the abstract bytecode comprises abstract routing information that indicates in an abstract coordinate system, which channel segments are used for connecting ports of the abstract logic blocks, wherein the configurable part of the client specific device comprises local logic blocks and a local routing architecture for connecting part of the local logic blocks, and wherein transforming the abstract bytecode into native bytecode comprises mapping the abstract logic block into the local logic blocks (Killian, 46:20 – 30).

Regarding claim 16, the method of claim 1, additionally comprising generating a virtual hardware/software interface that is representative of a class of hardware/software interfaces, the virtual hardware/software interface comprising a virtual hardware interface and virtual software interface (Shaylor, 9: 47 – 58).

Regarding claim 17, the method of claim 16, wherein executing the application on the client specific device comprises invoking a hardware/software interface, wherein the hardware/software interface comprising a virtual hardware/software interface and a local hardware/software interface that is specific for the client specific device (Shaylor, 5: 42 – 50).

Regarding claim 18, the method of claim 17, wherein the software bytecode communicates only with the virtual software interface, wherein the virtual software interface communicates with the local hardware/software interface, wherein the client specific device communicates only with the virtual hardware interface, and wherein the

virtual hardware interface communicates with the local hardware/software interface (Shaylor, 5: 42 – 50).

Regarding claim 19, which recites similarly to claim 5 as applied in claim 4, see reasoning as previously discussed above.

Regarding claim 20, which recites similarly to claim 8, see reasoning as previously discussed above.

Regarding claim 23, which recites similarly to claim 5, see reasoning as previously discussed above.

Regarding claim 24, which recites similarly to claim 8, see reasoning as previously discussed above.

Regarding claim 28, which recites the program storage version of claim 8, see reasoning as previously discussed above.

7. Claims 14, 15, 25, 26 and 29 are rejected under rejected under 35 U.S.C. 103(a) as being unpatentable over Shaylor USPN 6,760,907 B2 as applied in claim 1, in view of Williams USPN 6,631,508 B1.

Regarding claim 14, Shaylor discloses all the claimed limitations as applied in claim 1 above. Although, Shaylor doesn't explicitly disclose generating an application programming interface description, Shaylor does disclose converting the bytecodes into native code for the user's specific type of hardware (5: 57 – 60).

However, Williams does disclose this in an analogous art and similar configuration an API where the device is a FPGA (23:7 – 11). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Shaylor and Williams, because it would have enable the specific device to be configured more efficiently.

Regarding claim 15, the method of claim 14, Killian further discloses wherein executing the application comprises compiling at least the application programming interface description and executing the compiled application programming interface description, thereby generating the bit streams for reconfiguring the configurable part of the client specific device (Shaylor, 5: 57 – 60).

Regarding claim 25, which recites similarly to claim 14, see reasoning as previously discussed above.

Regarding claim 26, which recites similarly to claim 15, see reasoning as previously discussed above.

Regarding claim 29, which recites the program storage version of claim 15, see reasoning as previously discussed above.

Response to Arguments

8. Applicant's arguments,see page 2, or Applicant's response filed 04/04/05, with respect to claims 14, 15, 25, 26 and 29 have been fully considered and are persuasive. The rejection of 12/02/04 has been withdrawn.

However, regarding Applicant's argument in claims 1 – 4, 21, 22, 27 & 30 that Shaylor doesn't teach or disclose "executing the native bytecode at the client peer on the client specific device", Examiner still believes Shaylor does disclose this limitation (please see Shaylor, 5:55 – 65).

Shaylor discloses, "converting bytecodes into native code for the user's specific type of hardware 102 and operating system" (Emphasis added). Examiner interprets this to be configuring the client device. Applicant's plain language of claim merely calls for "configuring the configurable part of the client specific device", and hence this is taught by Shaylor.

Conclusion

9 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuck Kendall whose telephone number is 571-2723698. The examiner can normally be reached on 10:00 am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on 571-2723695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CK.

WEI Y. ZHEN
PRIMARY EXAMINER